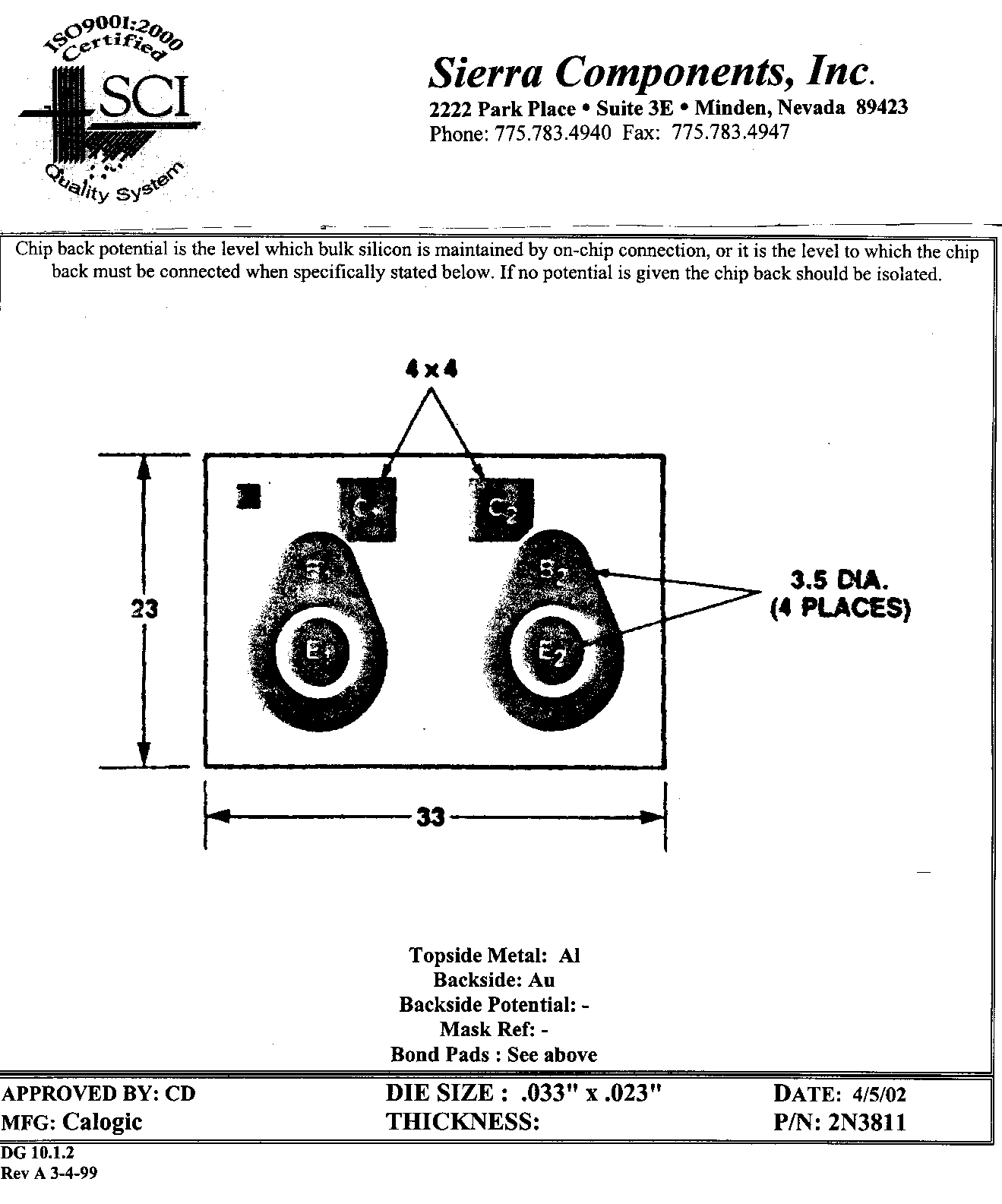
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

****

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: See Above**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .023” X .033” DATE: 10/18/21**

**MFG: CALOGIC THICKNESS .008” P/N: 2N3811**

**DG 10.1.2**

#### Rev B, 7/19/02